

DRAFT

Project COVER

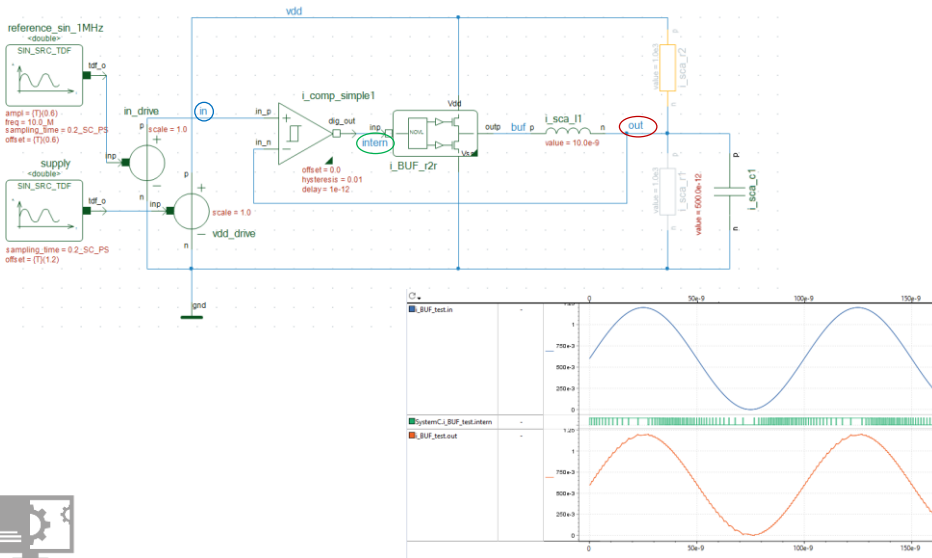
ISCD internship project, 24.7.2020

What does COVER stand for

- CO-VERification – for top-down design
 - Overall approach to verify design models based on system models
 - and
- COVER all angles – for use case verification
 - From system level down to design level



Working base / starting point: Class-D power amplifier with feedback

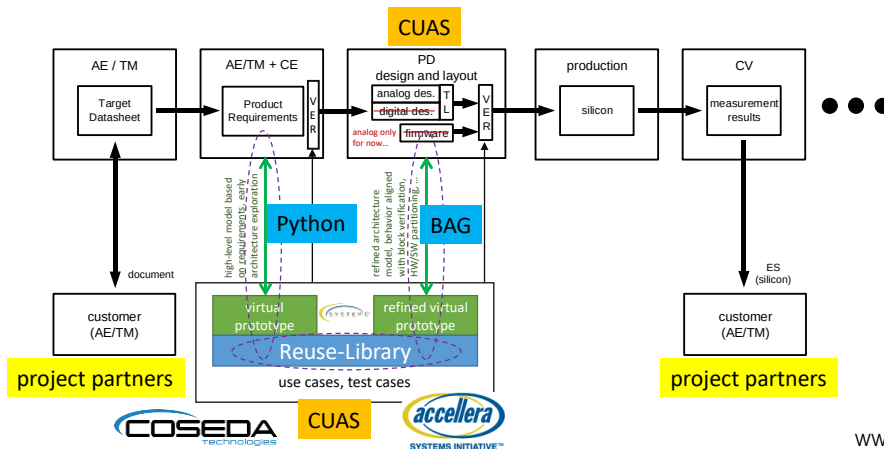


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(redrawn and modified) from: Simon Hainz, Infineon Technologies AG,
NASCUG Conference 2012

R&D design flow – based on IEEE1666.1 & BAG

• Project COVER



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3 columns the project build upon

- Modelling setup with automation – from concept level to design level

- **System level reuse** library with automated test setups

Coside
SystemC-AMS
Python

- Building blocks with proper parameters and individual test setups
- Must collaborate with top-down and bottom-up levels
- Automated test of library blocks (e.g. when compiling for future SC versions)



- Use **case development** connecting the abstract model with the design

Coside
SystemC-AMS
Python

- Supports to define the reuse library/model from to-down perspective
- Tests building blocks in a practical example
- Automated use case testing



- **Design verification** providing data to/from the abstract model

Cadence/BAG
SystemC-AMS
Python

- Supports to define the reuse library/model from a bottom-up perspective
- Simulate design blocks for system model calibration (bottom-up)
- Automated verification of design blocks based on a system model (top-down)



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Further readings

- SystemC/SystemC-AMS:
<https://www.accellera.org/activities/working-groups/systemc-ams>
- Coside:
<https://www.coseda-tech.com/coside-features>
- Python, PyCharm:
<https://www.python.org/>
<https://www.jetbrains.com/pycharm/>
- BAG:
<https://www2.eecs.berkeley.edu/Pubs/TechRpts/2019/EECS-2019-23.html>
- Class-D loop-back amplifier principle:
<https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=921936>

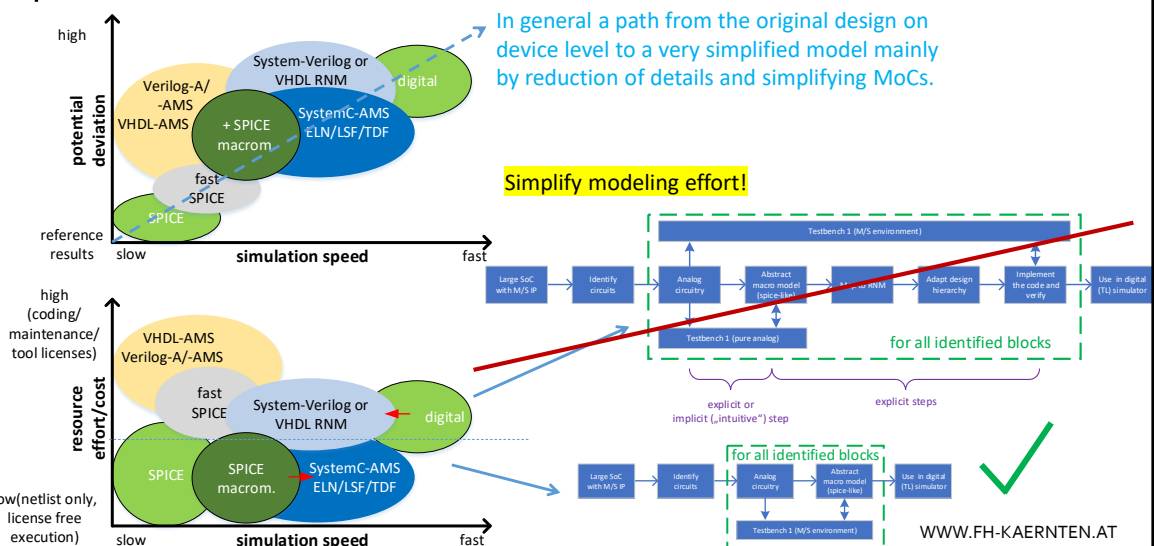


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Backup

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M/S modelling approaches - a qualitative view

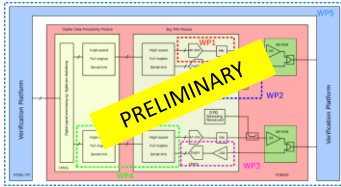


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SystemC-AMS at CUAS

Potential research topics (and Master Thesis topics):

- Modeling of analog RF (started in **RFFE-Lab**)



- Modeling of sensor systems (started in **Capsize**)
- Top-down methodology together with **BAG** (Berkeley Analog Generator)
- SystemC-AMS and HDLs like VHDL and SV
- SystemC-AMS and OpenModelica (<https://www.openmodelica.org/>)
- SystemC-AMS and FMI – functional mock-up interface (<https://fmi-standard.org/>)

