



MASTER THESIS - SAR ADC COMPARATOR LAYOUT GENERATOR DESIGN IN 28 NM TSMC TECHNOLOGY

RF SYSTEMS
VILLACH/LINZ/GRAZ/



In this master thesis new design methodology will be used for SAR ADC comparator layout generator design in 28nm TSMC technology. The candidate will familiarize himself/herself with the design framework (based on BAG (Berkeley Analog Generator)) with Python as a scripting tool and Cadence as a generator execution tool (co-supervised). She/he will identify the needed blocks and propose comparator floorplan (supervised) and search through already available layout generators database. In addition the candidate will identify and analyze similar layout generators (self-learning) and adapt the most fitting layout generator scripts to fit proposed floorplan (execution). She/he will write his/her own script (from scratch) for missing blocks or interconnections towards successful competition of the comparator layout generator.

YOUR FUTURE RESPONSIBILITIES

- Literature (re)search regarding comparator designs.
- Literature (re)search regarding analog layout techniques.
- Coded comparator layout generator within BAG framework.
- Publication of the results at a conference or in a scientific journal.

YOUR PROFILE

- Experience in Cadence analog design flow (from schematic to post-layout simulation).
- Python knowledge.
- Linux knowledge is a plus.
- Team player, self-motivated and goal oriented.

IMPORTANT FACTS

The starting date of this position is flexible.

This position is endowed with a gross monthly salary of € 1000,-/ for 15/h a week based on the collective agreement for research („Forschungs-Kollektivvertrag“).

The weekly hours are flexible and we are happy to discuss further options.

The contract is valid for 7 months.

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