



MASTER THESIS - TRANSIMPEDANCE AMPLIFIER LAYOUT GENERATOR DESIGN IN 28NM TSMC TECHNOLOGY

RF SYSTEMS
LINZ/VILLACH/GRAZ

In this master thesis new design methodology will be used for a Transimpedance amplifier (TIA) layout generator design in 28nm TSMC technology. The candidate will familiarize himself/herself with the design framework based on Berkeley Analog Generator (BAG) with Python as a scripting tool and Cadence as a generator execution tool (co-supervised). She/he will search through already available layout generators database and select the most fitting TIA layout generator (specifications vs. technology, control bits, etc.). The candidate will propose TIA floorplan (supervised) and analyze and adapt selected layout generators to fit proposed floorplan (execution). She/he will write his/her own script (from scratch) for missing blocks or interconnections towards successful completion of the TIA layout generator.

YOUR FUTURE RESPONSIBILITIES

- Literature (re)search regarding TIA designs.
- Literature (re)search regarding analog layout techniques.
- TIA layout generator coding within BAG framework in 28nm TSMC technology.
- Publication of the results at a conference or in a scientific journal.

YOUR PROFILE

- Experience in Cadence analog design flow (from schematic to post-layout simulation).
- Python knowledge.
- Linux knowledge is a plus.
- Team player, self-motivated and goal oriented.

IMPORTANT FACTS

The starting date of this position is flexible.

This position is endowed with a gross monthly salary of € 1000,-/ for 15/h a week based on the collective agreement for research („Forschungs-Kollektivvertrag“).

The weekly hours are flexible and we are happy to discuss further options.

The contract is valid for 7 months.

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